The Invention Claimed Is:

1. A programmable logic device comprising:

a plurality of input/output pins, each of which is configurable for use as an output pin or an input pin, and includes an associated tri-state driver with a data input terminal and an output enable terminal;

a plurality of regions of programmable logic, each of which includes a register having a clock signal input terminal, a data signal input terminal, and a data signal output terminal and configured to respond to a clock signal applied to the clock signal input terminal by applying to the data signal output terminal a data output signal indicative of the signal concurrently applied to the data signal input terminal;

a clock signal input pin connected to the clock signal input terminals of the registers; and

means for selectively coupling a data signal output terminal of a selected register to the data input terminals of the associated tri-state drivers of a subset of the input/output pins with fast conductors so that delay between application of a clock signal to the clock signal input pin and application of a data output signal from each input/output pin in the subset of the input/output pins indicative of the signal applied to the data signal input terminal of the selected register is within the PCI TCO time interval.

2. A programmable logic device comprising:

a plurality of input/output pins, each of which is configurable for use as an output pin or an input pin, and includes an associated tri-state driver with a data input terminal and an output enable terminal;

a plurality of regions of programmable logic, each of which includes a register having a clock signal input terminal, a data signal input terminal, and a data signal output terminal and configured to respond to a clock signal applied to the clock signal input terminal by applying to the data signal output terminal a data output signal indicative of the signal concurrently applied to the data signal input terminal;

a clock signal input pin connected to the clock signal input terminals of the registers; and

means for selectively coupling a selected input/output pin to the data signal input terminals of a subset of the registers with fast conductors so that delay between application of a clock signal to the clock signal input pin and application of a data input signal from the selected input/output pin to the data signal input terminals of the subset of the registers is within the PCI TSU time interval.

3. A programmable logic device comprising:

a plurality of input/output pins, each of which is configurable for use as an output pin or an input pin, and includes an associated tri-state driver with a data input terminal and an output enable terminal;

a plurality of regions of programmable logic, each of which includes a register having a clock signal input terminal, a data signal input terminal, and a data signal output terminal and configured to respond to a clock signal applied to the clock signal input terminal by applying to the data signal output terminal a data output signal indicative of the signal concurrently applied to the data signal input terminal;

a clock signal input pin connected to the clock signal input terminals of the registers; and

means for selectively coupling the data signal output terminal of a first selected register to the data input terminals of the associated tri-state drivers of a subset of the input/output pins and configured to selectively couple the data signal output terminal of a second selected register to the output enable terminals of the associated tri-state drivers of the subset of the input/output pins with fast conductors so that delay between application of a clock signal to the clock signal input pin and application of a data output signal from each input/output pin in the subset of the input/output pins indicative of the signal applied to the data signal input terminal of the first selected register is within the PCI TCZ time interval.